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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/670,833 | 09/25/2003 | Maximino Aguilar JR. | AUS920030706US1 | 8273 |

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| EXAMINER | |
|---|---|
| KAWSAR, ABDULLAH AL | |
| **ART UNIT** | **PAPER NUMBER** |
| 2109 | |
| **MAIL DATE** | **DELIVERY MODE** |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/670,833 | AGUILAR ET AL. | |
| | Examiner | Art Unit | |
| | Abdullah-Al Kawsar | 2109 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *03/02/2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1, 3-11,13-21 and 23-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-11,13-21 and 23-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *1/12/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *See Continuation Sheet*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Continuation of Attachment(s) 3). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :5/20/07,3/29/07,1/4/07,10/13/06,9/19/06,8/15/06,5/16/06,11/11/05,9/25/03.

## DETAILED ACTION

1. Claims 1, 2 - 11, 13 - 21 and 23 - 30 are pending. Claims 2, 12 and 22 are cancelled in the Preliminary Amendment dated 03/02/07.

### *Specification*

2. The use of the trademark "JAVA" has been noted in this application in specification page 13 lines 24. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

### *Claim Rejections - 35 USC § 112*

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 1, 11 and 21 are rejected under 35 U.S.C. 112, second paragraph, as being unclear and indefinite to particularly the subject matter which applicant regards as the invention. Claim 1 recites, ***"receiving a request from an application"*** but does not disclose specifically what type of request is being received. Examiner interprets the claim request as memory share request from first processor with a second processor.

6. Claims 11 and 12 are system and program product claims of claim 1 above. They are therefore rejected under the same rational.

***Claim Rejections - 35 USC § 101***

7. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 1, 3 - 11, 13 - 21 and 23 - 30 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The current focus of the Patent Office in regard to statutory inventions under 35 U.S.C. § 101 for method claims and claims that recite a judicial exception (software) is that the claimed invention recite a practical application. Practical application can be provided by a physical transformation or a useful, concrete and tangible result. No physical transformation is recited and additionally, the final result of the claims is a processing an application execution thread, which is not a tangible result because no actual computation is performed.

*Claim Rejections - 35 USC § 103*

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1, 3 – 6, 8 – 11, 13 – 16, 18 – 21, 23 - 26 and 28 - 30 are rejected under 35 U.S.C. 103(a) being unpatentable over Day et al (Day) US Patent No. 6981072 in view of Seino et al.(Seino) US Patent No. 5307495.

As per claim 1, Day discloses:

***- receiving a request from an application that is running on a first processor type; assigning one or more second processor types and a memory space to a group in response to the request, wherein the first processor type shares the memory space with the assigned second processor types, and wherein the first processor and the assigned second processor types are heterogeneous;*** (Col 2 lines 61-63, "The first processor 102 and the second processor 104 can have their own independent private virtual address space. Alternatively, they can share a virtual address space." And col 3 lines 9-10, "a block diagram 200 illustrates a preferred embodiment of a non-homogeneous multiprocessor system.") sharing memory between processors inherently means receiving a request from another processor to share a memory space.

However Day does not disclose, ***an application that is running on a first processor type and assigning one or more second processor types.***

On the other hand, Seino discloses:

***- an application that is running on a first processor type; assigning one or more second processor types*** ( col 5 lines 43-45, "When one of the processors of the system, for example, the processor 102 executes an instruction which requires communication among the processors") communicating with other processors means assigning one or more second processor.

Therefore, it would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Seino into the method of Day to assign one or more processor in response to an application. The modification would have been obvious because one of the ordinary skills of the art would use multiple processors with shared memory for processing efficiency and faster thread execution.

***- processing an application execution thread using the group, the application execution thread running on the first processor type and corresponding to the application.*** (Col 2 lines 63-67, "Objects in the system memory 114 referenced by an effective address in the first processor 102 part of the program can be referenced by the same effective address in the second processor 104 part of the program."), system memory is inherently accessed when an application is executing.

As per claim 3, the rejection of claim 1 is incorporated and further Day discloses:

***- identifying whether the application requests the memory space to be a private memory, wherein the private memory is accessible only by the assigned second processor types; and classifying the memory space as the private memory.*** (col 3 lines 62-67 "the second

MMU 220 can be programmed to respond to a translation lookaside buffer invalidate entry (TLBIE) instructions (e.g., PowerPC.TM. TLBIE) when using a common page table. Alternatively, the second MMU 220 can be programmed to ignore this instruction if using a private page table.").

As per claim 4, the rejection of claim 3 is incorporated and further Day discloses:

***- retrieving data from the private memory using one of the assigned second processor types; manipulating the data using one of the assigned second processor types, the manipulating resulting in resultant data; and storing the resultant data in a shared memory, the shared memory accessible by the first processor type.*** (col 3 lines 49-56, "This provides the capability for the SPU 214 to take advantage of the high performance access to its own private local storage, while still retaining aspects of a shared memory programming environment. Objects in the system memory 212 referenced by an effective address in the PU 202 part of the program can be referenced by the same effective address in the SPU 214 part of the program indirectly using DMA commands."), objects are the data in the system memory that can be accessed with both processor.

As per claim 5, the rejection of claim 1 incorporated and further Seino encloses:

***- retrieving an affinity selection bit from the application; determining whether the application requests affinity processor selection based upon the affinity selection bit; and performing the assigning using affinity processor selection.*** (col 6 lines 16-23, "A format of the PGID may be a 31-bit register having bit addresses 0-30. For example, when bit i (0-30) is at a

logical level "1", the processor i belongs to the processor group, and when it is at a logical level "0", the processor i does not belong to the processor group.").

As per claim 6, the rejection of claim 5 incorporated and further Seino encloses:

***- selecting one of the second processor types based upon the affinity processor selection; determining whether the selected second processor type is available; and performing the assigning based upon the selected second processor type's availability.*** (col 4 lines 51-58, "the processors are grouped and each group is assigned with a particular object of use. In each processor group, some virtual machine (VM's) are operated and an operating system (OS) which fits to the object of use is run on the VM's so that the object of use of the processor group is attained. The VM's are operated only in the processor group to which they belong.").

As per claim 8, the rejection of claim 1 incorporated and further Seino encloses:

***- wherein the group corresponds to one or more group properties, wherein the group properties are selected from the group consisting of a sharing mode, a priority, and a scheduling policy.*** (col 3 lines 18-22, "Group identification information is set to each processor. A processor which received an instruction which requires signaling identifies a group to which it belongs based on the group identification information assigned thereto").

As per claim 9, the rejection of claim 1 incorporated and further Day encloses:

***- wherein the group includes a plurality of second processors.*** (col 3 lines 22-23, "Similarly, there may be one or more additional processors (not shown), such as the SPC 210.").

As per claim 10, the rejection of claim 1 incorporated and further Day encloses:

***- wherein the first processor type is a processing unit and wherein the second processor types are synergistic processing units.*** ( col 3 lines 9-14, "The non-homogeneous multiprocessor system 200 comprises a processing unit (PU) 202 including an L1 cache 204, an L2 cache 206, a first MMU 208, a synergistic processor complex (SPC) 210, and a system memory 212. The SPC 210 includes a synergistic processor unit (SPU").

Claims 11, 13 - 16 and 18 - 20 are system claims of claims 1, 3 - 6 and 8 - 10 above. They are therefore rejected under the same rational.

Claims 22, 23 - 26 and 28 - 30 are computer program product claims of claims 1, 3 - 6 and 8 - 10 above. They are therefore rejected under the same rational.

11. Claim 7 is rejected under 35 U.S.C. 103(a) being unpatentable over Day et al (Day) US Patent No. 6981072 in view of Seino et al.(Seino) US Patent No. 5307495 and further in view of Ferrell et al.(Ferrell) US Patent No. 5630128.

As per claim 7, the rejection of claim 1 incorporated and further Seino encloses:

***- detecting that one or more of the second processor types are in use by an active execution thread;*** ( col 5 lines 43-45, "When one of the processors of the system, for example, the processor 102 executes an instruction which requires communication among the processors")

Neither Day nor Seino disclose, ***comparing the active priority to a requesting priority, the requesting priority corresponding to the application execution thread; and terminating the active execution thread if the active priority is lower than the requesting priority.***

On the other hand Farrell discloses:

***- identifying an active priority that corresponds to the active execution thread; comparing the active priority to a requesting priority, the requesting priority corresponding to the application execution thread; and terminating the active execution thread if the active priority is lower than the requesting priority.*** (col 6 lines 61-68, "the operating system service routine, which is executing on the currently executing program thread, is programmed to block the currently executing program thread in the following manner. The operating system service routine places itself onto a list of threads waiting on the queue, and then calls a Block primitive function 45 within the operating system to block its own thread." And col 6 lines 18-36, "Next the switch primitive function..... then the thread is executed from its beginning" and col 7 lines 18-21 "Next, the Block primitive function 44 calls the Switch primitive function 46 to select the highest priority thread on the run list for execution by the CPU")

Therefore, it would have been obvious to a person of ordinary skill in art at the time of invention was made to incorporate the teaching of Farrell into the combined method of Day and Seino to terminate an active thread to execute a higher priority thread. The modification would have been obvious because one of the ordinary skills of the art would execute priority thread for better and faster system overall performance and efficiency.

Claims 7, 17 and 27 are system and program product claims of claim 7 above. They are therefore rejected under the same rational.

***Conclusion***

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

TITLE: Multiprocessor system statically dividing processors into groups allowing processor of selected group to send task requests only to processors of selected group, US Patent No. 5,307,495.

TITLE: Memory management in multiprocessor system, US Patent No. 6,981,072 B2.

TITLE: Computer OS dispatcher operation with virtual switching queue and IP queues, US Patent No. 7,167,916 B2

TITLE: Parallel computer system and method for assigning processor groups to the parallel computer system, US PGPUB No. 2003/0045612 A1.

TITLE: Ring-topology based multiprocessor data access bus, US Patent No. 7,043,579 B2

TITLE: Controlled scheduling of program threads in a multitasking operating system, US 5,630,128

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abdullah-Al Kawsar whose telephone number is 571-270-3169. The examiner can normally be reached on 7:30am to 5:00pm, EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chameli Das can be reached on 571-270-1392. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Abdullah-Al Kawsar

Chameli Das

CHAMELI DAS
SUPERVISORY PATENT EXAMINER

6/7/07